Docket No.: 55123P256

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:

JUHA MIKKO HAKKARAINEN, ET AL.

Application No.: 10/624,794

Filed: July 22, 2003

For: **METHODS, SYSTEMS, AND APPARATUS FOR INTEGRATED CIRCUIT CAPACITORS IN CAPACITOR ARRAYS**

Art Group: Unassigned

Examiner: Unassigned

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In accordance with the duty of disclosure, enclosed is a copy of Information Disclosure Statement by Applicant (form PTO/SB/08), which is being submitted before the mailing of a first Office Action. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

It is hereby stated that no item of information contained in the Information Disclosure Statement was cited in a patent office in a counterpart application, and, to the knowledge of the undersigned, after making reasonable inquiry, no item of information contained in the Information Disclosure Statement was known to any individual associated with the filing or prosecution of the subject application more than three months prior to the filing of the Information Disclosure Statement.

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

Please charge any fees due to Deposit Account 02-2666. A duplicate copy of the Fee Transmittal (PTO/SB/17) is enclosed for this purpose.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: February 09, 2004

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I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Missing Parts, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Susan McFarlane — *02-09-04*

Susan McFarlane — ***Date***

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Sheet	1	of	2

Complete if Known	
Application Number	10/624,794
Filing Date	July 22, 2003
First Named Inventor	Juha Mikko Hakkarainen
Art Unit	Unassigned
Examiner Name	Unassigned
Attorney Docket Number	55123P256

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		BEHZAD RAZAVI, Design of Analog CMOS Integrated Circuits, pgs. 619-627, 637-462 and 650-653, McGraw-Hill Higher Education, ISBM 0071188150, 2001.	
		IURI MEHR & LARRY SINGER, A 55-mW, 10-bit, 40-Msample/s Nyquist-Rate CMOS ADC, pgs. 318-325, IEEE Journal of Solid-State Circuits, Vol. 35 No. 3, March 2002.	
		Lessons in Electrical Circuits, Vol IV (Digital), Chapter 13, http://www.ibiblio.org/obp/elecrticalcircuits/digital/digi_13.html, 4/2003.	
		B.RAZAVI & B.WOOLEY, A 12-b 5-MSample/s Two-Step CMOS A/D Converter, IEEE Journal of Solid-State Circuits, pgs. 1667-1678, Vol. 27 No. 12, December 1992.	
		THOMAS LEE, The Design of CMOS Radio-Frequency Integrated Circuits, pgs. 37-47, Cambridge University Press, Cambridge, UK, ISBN 0521630614, 1998.	
		D.ALLSTOT & W.BLACK, Technologyical Design Considerations for Monolithic MOS Switched-Capacitor Filtering Systems, pgs 967-986, Prod. of the IEEE, Vol 71 No 8, August 1983.	
		JAMES L. McCREARY, Matching Properties, and Voltage and Temperature Dependence of MOS Capacitors, pgs. 608-616, IEEE Journal of Solid-State Circuits, Vol. SC-16, No. 6, December 1981.	

Examiner Signature		Date Considered	

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

[1]Applicant's unique citation designation number. [2]Applicant is to place a check mark here if English language Translation is attached.

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Sheet	2	of	2

Complete if Known	
Application Number	10/624,794
Filing Date	July 22, 2003
First Named Inventor	Juha Mikko Hakkarainen
Art Unit	Unassigned
Examiner Name	Unassigned
Attorney Docket Number	55123P256

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Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		YANNIS TSIVIDIS & PAOLO ANTOGNETTI, Design of MOS VLSI Circuits for Telecommunications, pgs. 20-22, 314-333, Prentice-Hall, New Jersey, ISBN 013200643X01, 1985.	
		PAUL R. GRAY & ROBERT G. MEYER, Analysis and Design of Analog Integrated Circuits, Third Edition, pgs. 139-140, 167-170, John Wiley & Sons, Inc., ISBN 0471574953, 1993.	
		RAYMOND M. WARNER & JAMES N. FORDEMWALT, Integrated Circuits Design Principles and Fabrication, pgs. 246-255, 270, McGraw-Hill Book Company, 1965.	
		YOUNG-DEUK JEON, SEUNG-CHUL LEE, SANG-MIN YOO, & SEUNG-HOON LEE, Acquisition-Time Minimization and Merged-Capacitor Switching Techniques for Sampling-Rate and Resoulution Improvement of CMOS ADCs, pgs. 451-454, 2000 IEEE International Symposium on Circuits and Systems, 5/28-31, Geneva, Switzerland, 2000.	
		RICHARD C. DORF Editor-in-Chief, The Electrical Engineering, pgs. 15-33, 11321151, CRC Press, Boca Raton, FL, ISBN 0489301858, 1993.	
		DAVID HALLIDAY & ROBERT RESNICK, Physics Part Two Third Edition, 650-674, John Wiley & Sons, ISBN 948012, 1978.	
		ALAN B GRENENE, Bipolar and MOS Analog Integrated Circuit Design, pgs. 712-727, 753-764, 784-791, 825-879, ISBN 0471085294, John Wiley & Sons, Inc., 1984.	

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Based on PTO/SB/08B (08-03) as modified by Blakely, Sokoloff, Taylor & Zafman (wlr) 08/11/2003.
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